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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/783,246	02/13/2001	Michael D. Hutton	ALTRP061/A637	1693

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EXAMINER	
HOGAN, MARY C	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/783,246	HUTTON, MICHAEL D.	
	Examiner	Art Unit	
	Mary C Hogan	2123	

-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This application has been examined.

2. **Claims 1-30** have been examined and rejected.

Claim Interpretation

3. **Claim 2** is directed to "placing biased towards a state in which an individual path having a relatively high criticality is not changed so as to increase an associated delay". From the specification, it is discussed that the phase local will be adjusted to reflect the proportionate share of actual delays experienced in the most recent partitioning phase **(page 22, lines 24-25)** and in one case show an *increased delay* to reflect that actual observations from the most recent partition attempt where the delays from the cut were longer that previously estimated **(page 23, lines 1-6)**. From this explanation, it was determined that **Claim 2** was directed to partitioning based on using data from the placed design which includes an increased delay to reflect actual observations from the most recent partition attempt where the delays from the cut were longer that previously estimated.

4. **Claims 14-18, 20-23 and 25-29** are directed to "hierarchical type of cut" and "type of boundary". The specification states "For a hierarchical architecture, for h levels of hierarchy, the phase-local for phase "i" is defined to be a weighted average of the probabilistic delays of all stages I+1 to h" **(specification, page 19, lines 1-4)** and that local interconnect provides different units of delay based on what type of interconnect they are **(see specification, page 16 for example)**. From this explanation, it was determined that hierarchy is directed to "stages" which are functional block members connected together in a design. Further, it was concluded that and the "type of cut" or "type of boundary" refer to interconnect between the stages that are defined by the delay that they contribute to the path.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. **Claims 1-5, 8, 10, 11, 13, 19, 24 and 30** are rejected under 35 U.S.C. 102(e) as being anticipated by Hojat et al (U.S. Patent Number 6,080,201, excluding "Background of the Invention"), herein referred to as **Hojat A**.

7. As to **Claims 1,19,24 and 30**, **Hojat A** teaches: a method of estimating a critical path delay during a source electronic design placement into a target hardware device, comprising: receiving an electronic representation of the source electronic design **(column 7, lines 46-48 and 56-57)**; determining a path criticality in the source electronic design **(column 8, lines 50-61)** based on, determining an actual delay corresponding to a connection already placed across a first boundary in the target device **(column 8, lines 30-31, lines 54-60)**; determining a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary in the target device **(column 8, line 63-column 9, line 2)**; partitioning at least a portion of the source design by placing at least the portion of the source design across boundaries in the target device based on the determined actual delay and the statistical estimate for a future delay **(column 9, lines 7-10)**; determining a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary in the target device **(column 8, lines 63-67)** wherein partitions are still large and each partition contains "multiple placeable objects" which, when a future cut is made, the placer attempts to place these multiple objects as partitions become smaller **(column 11, lines 2-5)**; partitioning at least a portion of the source design by placing at least the portion of the source design across boundaries in the target device based on the determined actual delay and the statistical estimate for a future delay **(column 9, lines 7-10)**; a CPU and a user interface **(column 7, lines 39-46)**.

8. As to **Claim 2**, **Hojat A** teaches placing is biased towards a state in which an individual path having a relatively high criticality is not changed so as to increase an associated delay **(column 9, lines 7-10)** wherein net lengths queried from the placement state data are substituted for statistical net lengths.

9. As to **Claim 3**, **Hojat A** teaches the placing is biased towards a state in which an individual path having a relatively high criticality is changed in a manner that reduces the associated delay **(column 10, lines 21-26 and Figure 4B and description)**.

10. As to **Claim 4**, **Hojat A** teaches the estimate for the future delay is generated by performing partitioning techniques on at least one other electronic source design **(column 7, lines 48-50, 56-59)**, wherein the one other electronic source design is the initial placement and synthesis.

11. As to **Claims 5**, **Hojat A** teaches: the electronic representation is received in the form of hardware description language coding **(column 7, line 46)**.

12. As to **Claims 8, Hojat A** teaches the connections include at least one of conductive lines and switches **(column 4, lines 29-31)**.

13. As to **Claim 10, Hojat A** teaches iteratively repeating **(Figure 2, elements 204-216)** the determining a path criticality **(Figure 2B, element 208 and 210)** and the partitioning at least a portion of the source design **(Figure 2B, element 204)**.

14. As to **Claim 11, Hojat A** teaches determining whether to repartition the at least a portion of the source design after the partitioning **(column 9, lines 19-24 and 33-35)**; and if necessary, adjusting the estimates of delays from future partitions **(column 11, lines 1-2)** wherein estimated values that were used previously for unplaced portions of the design can be adjusted by using actual delays of objects that have now been placed.

15. As to **Claim 13, Hojat A** teaches adjusting the estimates of delays from future partitions comprises: substituting a percentage of delays attributed to the partition in the statistical estimate with a new percentage derived from the critical path delay results from the partition **(Figure 2B, repetition of elements 204-216 and column 11, lines 1-2)** wherein the new netlist is used that accounts for actual net lengths of newly placed elements in the design, thereby reducing the percentage of statistical estimates that are needed to model yet-unplaced portions of the design.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

18. **Claims 6,7 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hojat A** as applied to **Claim 1** above, and further in view of Lee (U.S. Patent Number 6,367,056), herein referred to as **Lee**.

19. As to **Claim 6 and7**, **Hojat A** teaches the electronic design representation is received in the form of a hardware description language and a netlist **(column 7, lines 46-47)**.

20. **Hojat A** does not expressly teach the electronic representation is received in the form of a schematic electronically captured.

21. **Lee** teaches the electronic design of an electronic device may exist in various states or stages such as a schematic **(column 5, lines 53-61)**.

22. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electronic design representations as taught in **Hojat A** to include a schematic representation since electronic design representations can exist in various states or stages as taught in **Lee (column 5, lines 53-61)**.

23. As to **Claim 9**, **Hojat A** teaches that the behavioral model is mapped to a "specific technology" that implements a design encoded in hardware description language **(column 14, lines 12-13, lines 62-64)**.

24. **Hojat A** does not expressly teach the target hardware device or "specific technology" is selected from a group comprising: a complex programmable logic device (CPLD), a field programmable gate array (FPGA), an application specific integrated circuit (ASIC), a programmable logic device, a general purpose microprocessor, and a board level circuit implementation.

25. **Lee** teaches the target hardware device is selected from a group comprising: a complex programmable logic device (CPLD) **(column 1, lines 27-28)**, a field programmable gate array (FPGA) **(column 1, line 26)**, an application specific integrated circuit (ASIC) **(column 1, lines 24-25)**, a programmable logic device **(column 1, lines 27-28)**, a general purpose microprocessor **(column 1, lines 23)**, and a board level circuit implementation **(column 6, line 12)** since these are examples of "target hardware devices" which implement an electronic design that may be encoded in a hardware description language **(column 5, lines 53-60)**.

26. It would have been obvious to one of ordinary skill in the art at the time the invention was made that the target hardware as taught in **Hojat A** could be chosen from a list containing CPLDs, FPGAs, ASICs, PLDs, general purpose microprocessors and board circuit level implementations since these are examples of "target hardware devices" which implement an electronic design that may be encoded in a hardware description language as taught in **Lee (column 5, lines 53-60)**.

27. **Claim12** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Hojat A** as applied to **Claims 1 and 11** above, and further in view of Hojat et al (U.S. Patent Number 6,080,201, "Background of the Invention"), herein referred to as **Hojat B**.

28. As to **Claim 12, Hojat A** teaches determining whether to repartition at least a portion of the source electronic design based on timing requirements **(column 9, lines 10-12, 39-42, column 10, 59-61)** wherein timing requirements must be met before the design in re-partitioned.

29. **Hojat A** fails to teach checking the timing requirements by comparing the critical path delays resulting from the partitioning cut with the estimate of critical path delays prior to the partitioning cut.

30. **Hojat B** teaches a method for determining whether a design meets timing criteria that determine whether to repartition at least a portion of the source electronic design by comparing the critical path delays resulting from the partitioning cut with the estimate of critical path delays prior to the partitioning cut wherein the "actual delay time" is the critical path delays resulting from the partitioning cut and "designed delay time" is the estimate of critical path delays prior to the partitioning cut **(column 3, line 61-column 4, line 5)** since the propagation delay time for a path as designed by the synthesizer is often different than the actual delay time of the path after the placement has placed it in the image **(column 3, lines 62-66)**.

31. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the checking timing requirements as taught in **Hojat A** with the checking of timing requirements as taught in **Hojat B** since the propagation delay time for a path as designed by the synthesizer is often different than the actual delay time of the path after the placement has placed the design in the image as taught in **Hojat B**.

32. **Claims 14-18, 20-23 and 25-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hojat A** as applied to **Claims 1,19,24 and 30** above, and further in view of Curtin et al (U.S. Patent Number 5,237,514), herein referred to as **Curtin**.

33. As to **Claims 14-18, 20-23 and 25-29, Hojat A** teaches: the statistical estimate for future delay comprises: receiving at least one source design **(column 7, lines 46-48 and 56-57)**; placing the at least one source design using partitioning methods to place the device across boundaries in the target device

(column 8, lines 19-25 and 30-32) and determining a statistical estimate for a future delay corresponding to an associated future connection to be placed across a second boundary in the target device **(column 8, line 63-column 9, line 2)**.

34. **Hojat A** does not expressly teach generating statistical data corresponding to each type of boundary crossed in the target device wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design, the statistical estimates correspond to the weighted average of the statistical data generated, the weighted average is based on a predetermined number or percentage of the slowest delays, or the weighted average is based on a predetermined number or percentage of the fastest delays.

35. As to **Claims 14,15,20,25 and 26, Curtin** teaches generating statistical data corresponding to each type of boundary crossed in the target device wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design **(column 5, lines 58-column 6, lines 11)** wherein the net segment slack constitutes the delay value of the type of cut and the contribution presence factor will provide the proportion of each hierarchical type of cut in the path. **Curtin** teaches this method to determine an approximation for an initial placement procedure that appropriately reflects the complexity of path interaction requirements and net slack tailoring in the positioning and partitioning of blocks **(column 5, lines 31-33 and 39-44)**.

36. As to **Claims 16,21 and 27, Curtin** teaches the statistical estimates correspond to the weighted average of the statistical data generated **(column 5, line 60 and lines 10-11)**.

37. As to **Claims 17,18,22,23,28 and 29**, it is concluded that the "net contribution factor" as taught in **Curtin** would allow the proportion, or percentage of fastest or slowest delays to be represented **(column 5, lines 60-63)**. Since these equations are solved to give a per "net segment" delay or slack contribution **(column 6, lines 22-24)**, it is determined that the contribution, or presence factor, "k" is a pre-determined value. Therefore, the weighted average as disclosed in **Curtin** is based on a predetermined number of the fastest and slowest delays.

38. It would have been obvious to one of ordinary kill in the art at the time the invention was made to modify the statistical estimate as taught in **Hojat A** with generating statistical data corresponding to each type of boundary crossed in the target device wherein the statistical data represents the proportion of each hierarchical type of cut of the entire number of cuts in the fully placed design as taught in **Curtin** since **Curtin's** method determines an approximation for the initial placement procedure that appropriately reflects the complexity of path interaction requirements and net slack tailoring in the positioning and partitioning of blocks **(column 5, lines 31-33 and 39-44)**.

Response to Arguments

39. Applicant's arguments filed on 12/3/04 regarding claims 1-30 have been considered but they are not persuasive.

40. Applicant argues: "..."Hojat does not teach or suggest determining a statistical estimate for a "future" delay corresponding to a "future" connection placed across a boundary" (page 9, paragraph 4).

41. As to the above argument, Hojat teaches determining a statistical estimate for a "future" delay corresponding to a "future" connection placed across a boundary" **(column 8, lines 63-67).** Hojat teaches this method with reference to **Figure 2B**. In this figure, Hojat teaches the cutting of the design and the subsequent timing analysis. Hojat uses statistical analysis to determine the net lengths for nets connecting objects in the same partition. When the process is repeated **(elements 204-216)**, the design is again "cut" and the objects connected in the same partition will now be separated into different partitions, therefore, the objects that were connected in the same partition are now connected across a boundary. Therefore, the statistical estimate used for the connection of objects inside the same partition is an estimate for a "future" delay corresponding to the "future" connection placed across a boundary that will occur when the circuit is cut again.

Conclusion

42. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C Hogan whose telephone number is 571-272-3712. The examiner can normally be reached on 7:30AM-5PM Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary C Hogan
Examiner
Art Unit 2123

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